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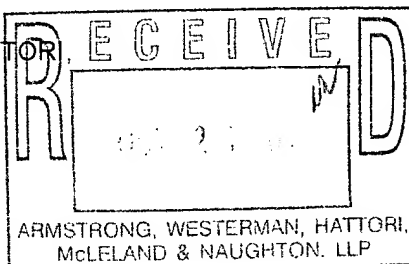
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/961,264	09/25/2001	2811	790	990355A	12	10	4

CONFIRMATION NO. 7825 ✓

23850

ARMSTRONG, WESTERMAN, HATTORI,
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1725 K STREET, NW, SUITE 1000
WASHINGTON, DC 20006



FILING RECEIPT



OC000000006938321

Date Mailed: 10/19/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Narumi Ohkawa, Kawasaki-shi, JAPAN;

Assignment For Published Patent Application

FUJITSU LIMITED, Kawasaki, JAPAN;

Domestic Priority data as claimed by applicant

THIS APPLICATION IS A DIV OF 09/288,302 04/08/1999

Foreign Applications

JAPAN HEI 10-281699 02/10/1998

10/02/1998 please correct date

If Required, Foreign Filing License Granted 10/19/2001

Projected Publication Date: 01/31/2002

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor device having both memory and logic circuit and its manufacture

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Preliminary Class

257

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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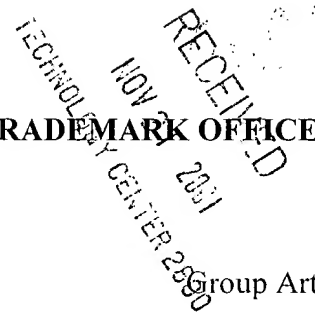
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In re the Application of: **Narumi OHKAWA**

Serial Number: **09/961,264**

Group Art Unit: **2811**

Filed: **September 25, 2001**

Examiner: **Not yet assigned**

For: **SEMICONDUCTOR DEVICE HAVING BOTH MEMORY AND LOGIC CIRCUIT
AND ITS MANUFACTURE**

REQUEST FOR CORRECTED FILING RECEIPT

Commissioner for Patents
Washington, D.C. 20231

November 13, 2001

Sir:

Please supply the undersigned attorney with a corrected filing receipt for the above-identified application. The undersigned also respectfully requests that the Patent and Trademark Office records be amended to reflect the correction.

In reviewing the official Filing Receipt, we noted an error in the date in the Foreign Application information. Please delete "02/10/1998" and insert --10-02-1998 --. A copy of the Claim for Priority which was filed in the parent application is enclosed.

We are enclosing a copy of the filing receipt with the corrections highlighted.

In the event that any fees are required in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON, LLP

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Enclosure: Copy of Filing Receipt & Copy of Claim for Priority